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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,558	03/30/2004	L. Gregory Meredith	MS1-4217US	1226

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LEE & HAYES, PLLC
601 W. RIVERSIDE AVENUE
SUITE 1400
SPOKANE, WA 99201

EXAMINER	
WANG, BEN C	

ART UNIT	PAPER NUMBER
2192	

NOTIFICATION DATE	DELIVERY MODE
05/27/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

lhptoms@leehayes.com

Office Action Summary	Application No.	Applicant(s)	
	10/816,558	MEREDITH ET AL.	
	Examiner	Art Unit	
	BEN C. WANG	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-10 and 45-53* is/are pending in the application.

4a) Of the above claim(s) *1-5 and 11-44* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-10 and 45-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is in response to the election filed on March 24, 2010.

2. Group 3 (claims 6-10, and 45-53) has been elected without traverse.

3. Claims 1-5, and 11-44 are withdrawn from consideration.

4. Claims 6-10, and 45-53 are pending.

Specification Objections

5. The specification is objected to because the following informalities:

- The use of trademarks, such as INTEL, has been noted in this application. Trademarks should be capitalized wherever they appear (capitalize each letter or accompany each trademark with an appropriate designation symbol, e.g., ™ or ®) and be accompanied by the generic terminology (use trademarks as adjectives modifying a descriptive noun). Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Drawing Objections

6. The drawings are objected to as failing to comply with 37 CFR t.84(p)(5) because they include the following reference character(s) not mentioned in the description:

- Duplicate label numbers (i.e., label numbers 202, 204, 206, and 208) used in both Figures 2A and 2B.
- Remove *DRAFT* label in all figures and non-use label numbers (300A and 302) in Figures 5A and 5B.

Corrected drawing sheets in compliance with 37 CFR 1.12 1 (d) are required in reply to the Office action to avoid abandonment of the application.

Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the Examiner, the Applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

7. Claims 6 and 45 are objected to because the following informalities:

- "… saving the result …", (in line 3 of claim 6 and line 4 of claim 45 respectively), should be corrected to read – a result --.
- "… the reflective process algebra …", (in line 5 of claim 45), should be corrected to read – a reflective process algebra --.

Claim Rejections – 35 USC § 103(a)

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 6-10 and 45-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leach et al. (Pat. No. US 6,625,719 B2) (hereinafter 'Leach') in view of Meredith et al. (Pub. No. US 2003/0212671 A1) (hereinafter 'Meredith')

9. **As to claim 6** (Original), Leach discloses a microprocessor for executing instructions (e.g., Col. 2, Lines 4-9 – 'microcomputer' and 'microprocessor' – both terms are used interchangeable; Fig. 1; Col. 3, Lines 29-30 - ... a microcomputer constructed according to the invention – emphasis added), comprising:

- a timing and control unit (e.g., Fig. 4, Instruction Decode and Control 202; Col. 2, Line 66 through Col. 3, Line 20 - … an instruction decode and control unit …) for retrieving an instruction from memory, decoding the instruction (e.g., … connected to the storage circuit and having an

instruction register operative to hold a program instruction is operative to decode the program instruction into control signals to control the operations of the data … - emphasis added), fetching data connected with the instruction (e.g., Col. 10, Lines 39 - 62 - … … two data fetches for operands and one data load), and saving the (a) result (e.g., Col. 11, Lines 10-14 - … The *dst* field 126 is decode by instruction decode and control 202 and signal *dst_select* is generated to select the destination register to store the result of the operation from ALU ... – emphasis added) and

- an arithmetic and logic unit (e.g., Col. 2, Line 66 through Col. 3, Line 20 - … an arithmetic control unit …) for performing an operation specified by the instruction (e.g., … operative to perform an arithmetic operation on data received by the arithmetic unit … - emphasis added)

Further, Leach discloses improvements which enhance interprocessor communications, and thus software and system development (e.g., Col. 2, Lines 59 - 63) and a variation of the parallel processing system architecture configuration (e.g., Col. 44, Lines 11 – 67) but does not explicitly disclose *the data including names obtained by literalizing processes in a reflective process algebra; and the instruction being expressed in a reflective process algebra, the reflective process algebra being capable of representing names as literalization of processes and processes as deliteralization of names*.

However, in an analogous art of *Operational Semantics Rules for Governing Evolution of Processes and Queries as Processes*, Meredith discloses a

programming language that can be used to define a sequence of instructions that can ultimately be processed and executed by a concurrent, distributed network of computing resources (e.g., [0002] – emphasis added) to overcome the problems associated with existing *π-calculus* and its variants in the prior arts (e.g., [0013] and [0015] – emphasis added; **NOTE**: the pending specification also articulates the same problem domain with *π-calculus*, for example, stated on all paragraphs in page 3 – emphasis added) and further teaches:

- the data including names obtained by literalizing processes in a reflective process algebra (Firstly, in light of the specification, lines 12 through 26 on page 7 - … The reflective process calculus causes *the dual nature* of a computation entity to be exposed. A *name* can be caused to become a *process* and a *process* can be caused to become a *name*. Thus, the reflective process calculus expresses the correspondence of the *dynamic* nature and the *static* nature of the computation entity … - emphasis added; Secondly, *Meredith* specifically states in the paragraph of [0044] - The term "process" used in accordance with the present invention means a *dynamic* representation of one or more computation entities that have the capability to evolve by performing actions or that allow other process to evolve … represents on of *a duality of natures* of a computation entity; [0017] - … for executing set of operational semantics rules governing the meanings of expression written in a *process-based* language … - emphasis added; Thus, *Meredith* indeed discloses the reflective process calculus as recited in the claim; [0044] - … when a computation entity is at

rest, it can be examined, such as by viewing a program *[interpreted as names as literalization of process]*); and

- the instruction being expressed in a reflective process algebra, the reflective process algebra being capable of representing names as literalization of processes and processes as deliteralization of names (e.g., [0044] - The term "process" used in accordance with the present invention means a *dynamic* representation of one or more computation entities that have the capability to evolve by performing actions or that allow other process to evolve … represents on of *a duality of natures* of a computation entity … when a computation entity is at rest, it can be examined, such as by viewing a program *[interpreted as names as literalization of process]*. When a computation entity is mobile (as a process), it can be seen, but its behaviors can be expressed and verified by a programming 400 formed in accordance with the present invention *[interpreted as processes as deliteralization of names]* – emphasis added)

Therefore, it would have been obvious to one of ordinary skill in the pertinent art, at the time the invention was made to combine the teachings of Meredith into the Leach's system to further provide other limitations stated above in the Leach system.

The motivation is that it would further enhance the Leach's system by taking, advancing and/or incorporating the Meredith's system which offers significant advantages for allowing processes in concurrent, distributed computing networks to interact while avoiding or reducing the foregoing and other problems

associated with existing π-calculus and its variants (e.g., [0016] – emphasis added) and further the invention is operational with numerous other general purpose or special purpose computing system environments or configurations including multiprocessor systems and microprocessor-based systems (e.g., [0032] – emphasis added) as once suggested by Meredith.

10. **As to claim 7** (Original) (incorporating the rejection in claim 6), Leach discloses the microprocessor further comprising a register array for storing the result of the executed instruction (e.g., Col. 25, Line 66 through Col. 26, Line 16 - … auxiliary registers … to the output FIFO of a communication port …).

11. **As to claim 8** (Original) (incorporating the rejection in claim 7), Leach discloses the microprocessor further comprising an instruction register and decoder for holding the instruction of the microprocessor is executing (e.g., Col. 3, Lines 5 – 14 - … an instruction register operative to hold a program instruction is operative to decode the program instruction … - emphasis added).

12. **As to claim 9** (Original) (incorporating the rejection in claim 8), Leach discloses the microprocessor further comprising bus connections for allowing the microprocessor to receive data into memory internally and for communicating result of the executed instruction externally (e.g., Col. 6, Lines 29 – 37 - External connection is made by way of peripheral ports 24 and 26, which multiplex various bus signals onto external terminals of microcomputer 10 and which provide

special purpose signals for communication to external device … - emphasis added).

13. **As to claim 10** (Original) (incorporating the rejection in claim 9), Leach discloses the microprocessor wherein the timing and control unit, the arithmetic and logic unit, and the instruction register and decoder communicates via ports that have unilateral contracts associated with ports (e.g., Col. 6, Lines 19 – 59 - .. … As is evident from Fig. 1, memories 16, 18 and 20 each have two ports 32a and 32d. Each of ports 32a … receive the address signals presented thereupon to provide access to the corresponding memory …).

14. **As to claim 45** (Original), Leach discloses an array of microprocessors for executing instructions (e.g., Fig. 22; Col. 43, Lines 48-55 – one possible system shown in Fig. 22 is a pipelined linear array using three microcomputer 10 … - emphasis added), comprising:

at least one microprocessor that includes one or more components:

- a timing and control unit (e.g., Fig. 4, Instruction Decode and Control 202; Col. 2, Line 66 through Col. 3, Line 20 - … an instruction decode and control unit …) for retrieving an instruction from memory, decoding the instruction (e.g., … connected to the storage circuit and having an instruction register operative to hold a program instruction is operative to decode the program instruction into control signals to control the operations of the data … - emphasis added), fetching data connected with the instruction (e.g., Col. 10, Lines 39 - 62 - … … two data fetches for

operands and one data load), and saving the (a) result (e.g., Col. 11, Lines 10-14 - … The *dst* field 126 is decode by instruction decode and control 202 and signal *dst_select* is generated to select the destination register to store the result of the operation from ALU ... – emphasis added); and

- an arithmetic and logic unit (e.g., Col. 2, Line 66 through Col. 3, Line 20 - … an arithmetic control unit …) for performing an operation specified by the instruction (e.g., … operative to perform an arithmetic operation on data received by the arithmetic unit … - emphasis added)

Further, Leach discloses improvements which enhance interprocessor communications, and thus software and system development (e.g., Col. 2, Lines 59 - 63) and a variation of the parallel processing system architecture configuration (e.g., Col. 44, Lines 11 – 67) but does not explicitly disclose *the data including names obtained by literalizing processes in the (a) reflective process algebra; and the instruction being expressed in a reflective process algebra, the reflective process algebra being capable of representing names as literalization of processes and processes as deliteralization of names.*

However, in an analogous art of *Operational Semantics Rules for Governing Evolution of Processes and Queries as Processes*, Meredith discloses a programming language that can be used to define a sequence of instructions that can ultimately be processed and executed by a concurrent, distributed network of computing resources (e.g., [0002] – emphasis added) to overcome the problems associated with existing *π-calculus* and its variants in the prior arts (e.g., [0013]

and [0015] – emphasis added; **NOTE**: the pending specification also articulates the same problem domain with *π-calculus*, for example, stated on all paragraphs in page 3 – emphasis added) and further teaches:

- the data including names obtained by literalizing processes in the (a) reflective process algebra (Firstly, in light of the specification, lines 12 through 26 on page 7 - … The reflective process calculus causes *the dual nature* of a computation entity to be exposed. A *name* can be caused to become a *process* and a *process* can be caused to become a *name*. Thus, the reflective process calculus expresses the correspondence of the *dynamic* nature and the *static* nature of the computation entity … - emphasis added; Secondly, *Meredith* specifically states in the paragraph of [0044] - The term "process" used in accordance with the present invention means a *dynamic* representation of one or more computation entities that have the capability to evolve by performing actions or that allow other process to evolve … represents on of *a duality of natures* of a computation entity; [0017] - … for executing set of operational semantics rules governing the meanings of expression written in a *process-based* language … - emphasis added; Thus, *Meredith* indeed discloses the reflective process calculus as recited in the claim; [0044] - … when a computation entity is at rest, it can be examined, such as by viewing a program *[interpreted as names as literalization of process]*) and
- the instruction being expressed in a reflective process algebra, the reflective process algebra being capable of representing names as

literalization of processes and processes as deliteralization of names (e.g., [0044] - The term "process" used in accordance with the present invention means a *dynamic* representation of one or more computation entities that have the capability to evolve by performing actions or that allow other process to evolve … represents on of *a duality of natures* of a computation entity … when a computation entity is at rest, it can be examined, such as by viewing a program *[interpreted as names as literalization of process]*. When a computation entity is mobile (as a process), it can be seen, but its behaviors can be expressed and verified by a programming 400 formed in accordance with the present invention *[interpreted as processes as deliteralization of names]* – emphasis added)

Therefore, it would have been obvious to one of ordinary skill in the pertinent art, at the time the invention was made to combine the teachings of Meredith into the Leach's system to further provide other limitations stated above in the Leach system.

The motivation is that it would further enhance the Leach's system by taking, advancing and/or incorporating the Meredith's system which offers significant advantages for allowing processes in concurrent, distributed computing networks to interact while avoiding or reducing the foregoing and other problems associated with existing π-calculus and its variants (e.g., [0016] – emphasis added) and further the invention is operational with numerous other general purpose or special purpose computing system environments or configurations

including multiprocessor systems and microprocessor-based systems (e.g., [0032] – emphasis added) as once suggested by Meredith.

15. **As to claim 46** (Original) (incorporating the rejection in claim 45), Leach discloses the array of microprocessors wherein the array of microprocessors are on a single integrated circuit (e.g., Col. 2, Lines 47 - 57 - … single-chip devices …).

16. **As to claim 47** (Original) (incorporating the rejection in claim 45), Leach discloses the array of microprocessors wherein the array of microprocessors are on multiple integrated circuits, the multiple integrated circuits being mounted on a single board (e.g., Col. 2, Lines 47 - 57 - … single systems …).

17. **As to claim 48** (Original) (incorporating the rejection in claim 45), Leach discloses the array of microprocessors wherein the array of microprocessors are on multiple integrated circuits, the multiple integrated circuits being mounted on multiple boards, the multiple boards being housed on a single rack of a computer (e.g., Col. 2, Lines 47 - 57 - … single systems …).

18. **As to claim 49** (Original) (incorporating the rejection in claim 45), Leach discloses the array of microprocessors wherein the array of microprocessors are on multiple integrated circuits, the multiple integrated circuits being mounted on multiple boards, the multiple boards being housed on multiple racks of multiple computers (e.g., Col. 44, Lines 34 – 38 - The flexibility from the various communication port connections and memory sharing capabilities of

microcomputers 10 provide systems .. using a single microcomputer 10 or multiple microcomputers 10).

19. **As to claim 50** (Original) (incorporating the rejection in claim 45), Leach discloses the array of microprocessors further comprising a network for coupling one or more microprocessors, the network being selected from a group consisting of permanent connections and temporary connections (e.g., Col. 37, Lines 24 – 30 - … coupled to microcomputer 10 via one or more or all the communication ports … the connection between two microcomputers 10 where one communication port is connected to the other communication port …; Fig. 19; Col. 43, Lines 14 – 31 - … connections to a plurality of memories … Microcomputer 10 also has available six communication channels capable of interfacing to other systems … - emphasis added).

20. **As to claim 51** (Original) (incorporating the rejection in claim 45), Meredith discloses the array of microprocessors wherein the components of the at least one microprocessor are synchronized by instructions produced by a compiler that compiles a program written in the reflective process algebra (e.g., [0030] - … illustrating an exemplary method formed in accordance with this invention for compiling a program via a compiler …; [0047] – The queue 310 through which processes communication can take various forms … suitable structures stores … communication means can be used to implement solutions for both asynchronous and synchronous scenarios requiring high performance … - emphasis added).

21. **As to claim 52** (Original) (incorporating the rejection in claim 45), Meredith discloses the array of microprocessors wherein the array of microprocessors are synchronized by instructions produced by a compiler that compiles a program written in the reflective process algebra (e.g., [0030] - … illustrating an exemplary method formed in accordance with this invention for compiling a program via a compiler …; [0047] – The queue 310 through which processes communication can take various forms … suitable structures stores … communication means can be used to implement solutions for both asynchronous and synchronous scenarios requiring high performance … - emphasis added).

22. **As to claim 53** (Original) (incorporating the rejection in claim 45), Leach discloses the array of microprocessors wherein the components of the at least one microprocessor lacks circuitry for predicting a next instruction to be executed (e.g., Col. 24, Line 39 through Col. 25, Line 15 - … This is a cache 'miss' … a cache 'miss' also occurs …).

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben C. Wang whose telephone number is 571-270-1240. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ben C Wang/
Examiner, Art Unit 2192

/CHAMELI C. DAS/
Primary Examiner, Art Unit 2192
Dated: 5/20/10